WE CLAIM:

1. An integrated circuit chip having active components on its active surface, comprising:

electrically non-functional metallic thermal conductors integrated on said active surface of said chip, and thermally conductively connected to one of said active components; and

the position of said conductors selected to enhance dissipation of thermal energy released from said active components below said conductors.

2. An integrated circuit chip having active components on its active surface, comprising:

metallic lines having a thermal conductance at least an order of magnitude greater than underlying thin film electrical interconnects, integrated on said active surface;

means for connecting said lines to an outside heat sink; and

said lines and said connecting means positioned to steepen the temperature gradient for thermal flux from one or more selected active components to the corresponding line and said sink, to which said flux is to be delivered.

3. An integrated circuit chip having active components on its active surface, comprising:

a metal network of electrical power distribution lines, said lines having a thermal conductance at least an order of magnitude greater than underlying thin film electrical interconnects, deposited on the surface of said chip, located directly over said active components;

said lines electrically and thermally connected vertically to selected active components below said lines;

electrical conductors operable to connect said lines to an outside source; and

additional, electrically non-functional conductors distributed on said lines, operable to steepen the temperature gradient for thermal flux away from said active components and lines.

4. A semiconductor device having an additional conductor network on the chip surface, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer;

conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable;

said network patterned to spread thermal energy and distribute electrical power current and ground potential;

electrical conductors connecting said network lines to an outside electrical source; and

additional thermal-only conductors distributed on

said lines for thermal flux away from said lines to an outside heat sink.

5. The device according to Claim 4 further comprising:

a plurality of windows opened in said chip overcoat to expose circuit contact pads;

a leadframe having a chip mount pad, a first plurality of segments providing electrical power and ground and a second plurality of segments providing electrical signals;

said second chip surface attached to said chip mount pad;

electrical and thermal conductors connecting said network lines with said first plurality of segments; and

electrical conductors connecting said chip contact pads with said second plurality of segments.

6. The device according to Claim 5 wherein said electrical and thermal conductors are bonding wires or ribbons.

7. The device according to Claim 4 further comprising:

a substrate having a plurality of bondable and solderable electrical contact pads;

a heat sink integral with said substrate, said sink thermally connected to said contact pads; and

electrical and thermal conductors connecting said chip network lines and said substrate contact pads.

8. The device according to Claim 7 wherein said electrical and thermal conductors are solder balls or bumps.

9. The device according to Claim 4 wherein said chip is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electronic

device fabrication.

10. The device according to Claim 4 wherein said circuit comprises a plurality of active and passive electronic components arranged horizontally and vertically.

11. The device according to Claim 4 wherein said integrated circuit comprises multi-layer metallization, at least one of said layers made of pure or alloyed copper, aluminum, nickel, or refractory metals.

12. The device according to Claim 4 wherein said overcoat comprises materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide, and sandwiched films thereof.

13. The device according to Claim 5 wherein said leadframe is pre-fabricated from a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar.

14. The device according to Claim 6 further comprising an encapsulation enclosing said chip, chip mount pad, electrical conductors, and at least portions of said first and second plurality of leadframe segments.

15. The device according to Claim 14 wherein said encapsulation comprises a transfer molding process using a polymer compound with thermally conductive fillers.

16. The device according to Claim 4 wherein said conductive films comprise at least one stress-absorbing metal layer selected from a group consisting of copper, nickel, aluminum, tungsten, titanium, molybdenum, chromium, and alloys thereof.

17. The device according to Claim 4 wherein said outermost metal layer is selected from a group consisting of pure or alloyed gold, palladium, silver, platinum, and

aluminum.

18. The device according to Claim 6 wherein said bonding wire is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

19. The device according to Claim 8 wherein said solder ball is selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

20. The device according to Claim 4 wherein said network of lines, together with said metal-filled vias, provides the power distribution function between said active circuit components.

21. A method for fabricating a semiconductor device including a semiconductor chip having first and second surfaces, comprising the steps of:

forming an integrated circuit on said first chip surface, said circuit including active components, at least one metal layer, and a mechanically strong, electrically insulating protective overcoat;

forming a plurality of vias through said overcoat to access said at least one metal layer;

filling said vias by depositing a stack of metal films on said overcoat, said stack having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable;

patterning said films into a network of lines such that said lines are located substantially vertical over said active components and are suitable for heat dissipation;

forming a plurality of windows in said overcoat to expose circuit contact pads;

attaching electrical conductors operable to connect said lines to an outside source;

attaching additional thermal-only conductors, distributed on said lines, operable to steepen the temperature gradient for thermal flux away from said active components and lines; and

attaching electrical conductors to said circuit contact pads.

22. The method according to Claim 21 further comprising the steps of:

providing a pre-fabricated leadframe comprising a chip mount pad, a first plurality of segments suitable for electrical signals, and a second plurality of segments suitable for electrical power and ground; .

attaching said chip to said chip mount pad;

attaching said electrical conductors attached to said circuit contact pads to said first plurality of segments; and

attaching said electrical conductors attached to said lines to said second plurality of segments.

23. The method according to Claim 21 wherein said steps of attaching thermal and electrical conductors to said lines and contact pads comprise either the steps of attaching bonding wires or ribbons, or the steps of reflowing solder balls.

24. The method according to Claim 22 further comprising the step of encapsulating said chip, chip mount pad, thermal and electrical conductors and at least a portion of said leadframe segments in a package.